

CLAIMS:

1. An opto-electronic device, comprising:
 - a semiconductor substrate;
 - a photodetector formed adjacent the semiconductor substrate; and

5 a capacitor formed adjacent the semiconductor substrate, wherein said capacitor is coupled between a photodetector AC ground and a photodetector bias terminal.

10 2. The opto-electronic device of claim 1 wherein the capacitor comprises an insulator layer formed adjacent to a first electrode and a conductive layer formed adjacent to said insulator layer and overlapping a portion of said first electrode.

15 3. The opto-electronic device of claim 2 wherein the first electrode comprises a region of conductive semiconductor material.

20 4. The opto-electronic device of claim 2 wherein the first electrode comprises a metal layer.

5. The opto-electronic device of claim 2 wherein the insulator layer comprises a dielectric layer.

25 6. The opto-electronic device of claim 5 wherein the dielectric layer comprises silicon nitride.

30 7. The opto-electronic device of claim 5 wherein the dielectric layer comprises silicon dioxide.

8. The opto-electronic device of claim 2 wherein the dielectric layer comprises silicon oxynitride.

9. The opto-electronic device of claim 5 wherein the dielectric layer comprises an organic dielectric.

10. The opto-electronic device of claim 5 wherein the
5 dielectric layer comprises an inorganic dielectric.

11. The opto-electronic device of claim 2 wherein the photodetector comprises a metal-semiconductor-metal detector.

10 12. The opto-electronic device of claim 2 wherein the photodetector comprises an avalanche photodiode.

13. The opto-electronic device of claim 2 wherein the photodetector comprises a photodiode.

14. The opto-electronic device of claim 13 wherein said photodiode comprises:

an intrinsic layer sandwiched between an n-type layer and a p-type layer.

15. The opto-electronic device of claim 14 wherein an isolating implant region is formed in a first portion of said n-type layer.

25 16. The opto-electronic device of claim 15 wherein said isolating implant region comprises a proton implant region.

17. The opto-electronic device of claim 15 wherein said first electrode comprises a photodetector n-type ohmic contact
30 deposited adjacent said n-type layer, and wherein the second electrode overlaps at least a portion of said first electrode.

18. The opto-electronic device of claim 1 further comprising a bias resistor, wherein said bias resistor couples
35 said photodetector to said bias terminal.

19. An opto-electronic device, comprising:

an array of photodetectors, wherein one or more monolithic capacitors capacitively couple one or more of the photodetectors to one or more bias terminals.

5

20. The opto-electronic device of claim 19 wherein a single monolithic capacitor couples a plurality of said photodetectors to a single bias terminal.

10

21. The opto-electronic device of claim 19 wherein a plurality of monolithic capacitors couple a plurality of said photodetectors to said one or more bias terminals.

DRAFT
ENTRANCE
TO THE
PATENT
OFFICE

15 22. The opto-electronic device of claim 19 further comprising one or more bias resistors, wherein said one or more bias resistors couple said one or more photodetectors to said one or more bias terminals.

20 23. The opto-electronic device of claim 19 wherein a separate monolithic capacitor individually couples each of said one or more photodetectors to said one or more bias terminals.

25

24. The opto-electronic device of claim 19 further comprising a plurality of monolithic bias resistors, wherein a separate bias resistor is coupled between each of said one or more photodetectors and said one or more bias terminal.

30

25. The opto-electronic device of claim 19 further comprising a monolithic bias resistor coupled between said one or more photodetectors and a single bias terminal.

26. The opto-electronic device of claim 19 wherein each of said one or more capacitors comprises a dielectric layer formed adjacent to a first electrode and a conductive layer formed

adjacent to said dielectric layer and overlapping a portion of said first electrode.

27. The opto-electronic device of claim 22 wherein said one or more bias resistors each comprise a conductive resistor layer formed adjacent a conductive portion of an otherwise electrically isolated region.

28. The opto-electronic device of claim 27 wherein said conductive resistor layer is formed on a mesa structure.

29. The opto-electronic device of claim 27 wherein said isolated region comprises an implant region, and wherein said implant region laterally isolates said conductive resistor layer.

30. An opto-electronic device; comprising:
a multilayered VCSEL formed on a substrate;
a photodetector formed laterally adjacent to said VCSEL substrate; and

a capacitor formed on a surface of said photodetector, wherein said capacitor is coupled between a photodetector AC ground and a photodetector bias terminal.

31. The opto-electronic device of claim 30 wherein the capacitor comprises a dielectric layer formed adjacent to a first portion of a first electrode and conductive layer formed adjacent to said dielectric layer and overlapping a second portion of said first electrode.

32. The opto-electronic device of claim 30 wherein the photodetector comprises a photodiode.

33. The opto-electronic device of claim 30 wherein the photodetector comprises a metal-semiconductor-metal detector.

34. The opto-electronic device of claim 30 wherein the photodetector comprises an avalanche photodiode.